EE 330 Coverage - Fall 2007

		Topics
Week	1	
	1	Electronic Systems Overview, Economic Opportunities
	2	Yield and Cost of Semiconductor Products
	3	Physical characteristics, soft faults
Week	2	
	4	Digital Systems - Basic Gates, Switch-Level MOS Models
	5	Digital Systems - Complex Logic Gates, Pass Transistor Logic, Improved Switch-Level MOS Model
	6	Paramater Extraction for Imp. Switch-Level Model, Propagation Delay in Logic, Placement, Stick Diagrams
Week	3	
		Holiday
	7	Technology Files, Design Rules, Layout
	8	Fabrication Technology, Processing Steps
Week	4	
	9	Fabrication Technology, Processing Steps
	10	Interconnects - resistive and capacitive
	11	Backed Technology - Packaging, Bonding, Basic Semiconductor Processes
Week	5	
	12	Devices/Device Models in Semiconductor Proceses - Resistors, Diodes
	13	Diode Operation, Diode Model (Diode Equation), simplified diode models
	14	Diode Applications, Capacitor types and Models, MOSFET operation
Week	6	
	15	MOSFET Operation - square law model, short channel model, BSIM model (brief)
	16	MOS Process Description - (n-channel, p-channel, capacitors, resistors)
	17	Exam 1
Week	7	
	18	Small feature MOS processes, Bipolar Devices and operation
	19	Bipolar Devices - operation, device model, simplified device model
	20	Bipolar Process Description - (vertical and lateral devices, JFET, diffused resistor, varactor, diode)
Week	8	
	21	MOS and Bipolar Device Comparisons, Q-point calculation
	22	Transistors as Amplifiers (MOS and Bipolar)
	23	Small-signal principles, ss models of 2-terminal devices, ss diode model
Week	9	
	24	Small-signal models of 3-terminal and 4-terminal devices, small signal MOSFET model
	25	Small-signal BJT models, small siignal ciruit analysis, load lines, signal swings
	26	MOSFET Model Extension (Bulk htreshold), Comparison of MOS and Bipolar devices t as amplifiers, Dependence of SS paramaters on Q-poin
Week	10	
	27	Basic Amplifier Structures-CS/CE, CD/CC, CG/CB
	28	Basic Amplifier Structures-CS/CE, CD/CC, CG/CB
	29	High Gain Amplifies- Cascoding
Week	11	
	30	High Gain Amplifiers - Cascoding, Cascading
	31	Current Source Biasing, Darlington Configuration
	32	Current Sources and Mirrors
Week	12	
	33	Differential Amplifiers (brief), Bipolar and MOS Mappings
	34	Heirarchiacal Digital Design - Behavioral, Structural, Physical, Digital Design Flows
	35	Basic Gates, Charatristics of Logic Families, the Inverter Pair
Week	13	
	36	Analyysis of Logic Circuits (at transistor level), VH, VL, VTRIP, Static I/V Char of CMOS Inverter, Inverter Device Sizing
	37	Other CMOS Logic (ration logic), Propagation Delay in Static CMOS, Logic Gate Device Sizing, Reference Inverters
	38	Propagation Delay in Multiple Levels of Logic, Overdrive
Week	14	
	39	Asymmetric Overdrive and Propagation Delay, Driving large capacitive loade
	40	Pad Drivers, Logical Effort, Elmore Delay, Ring Oscillators
	41	Exam 2
Week	15	
	42	Complex Logic Gates, Pass Transistor Logic, Pseudo NMOS, Dynamic Logic (Domino and Zipper)
	43	Sequential Logic - Latches, Flip Flops, Shift Registers, Array Logic, Sea of Gates and Gate Arrays
	44	Memory Structures - Row/Colum Decoders, Mem Cells (SRAM, DRAM, SROM, EEPROM) High Frequency MOS Model (not enough time to cover)